REMARKS

This amendment is submitted in response to the Office Action dated April 11, 2007. Reconsideration and allowance of the claims are requested. In the Office Action, claim 1 was rejected as being indefinite. Therefore, the claim has been reviewed and edited to eliminate this issue.

Claims 1-8, 10 and 12-20 stand rejected under 35 USC §102(b) as anticipated by Wilson (US 5,557,734). Claim 9 is rejected under 35 USC §103(a) as obvious over Wilson in view of Okuda (US 6,535,452). Claim 11 is rejected under 35 USC §103(a) as obvious over Wilson considered with "Computer Organization and Design" (hereinafter "Hennessy") with Hennessy being offered as evidence of general design concepts in the field of data cache design.

These rejections are respectfully traversed. Claim 1 has been edited to incorporate the limitations of claim 22 and to clarify the operation of the reconfigurable execution node RXN. The RXN is operable and configurable to perform any one of the number of desired operations in response to control words stored in the cache memory. A reconfigurable execution node, as claimed herein, is not shown anywhere in the Wilson reference, which discloses only a fixed operation processor. The Examiner relies on a truth table processor 46, shown in detail in Figure 7, a max value processor 47, shown in detail in Figure 8, and a numeric processor 48, shown in detail in Figure 9. All these processors are defined by hard wire logic, and do not comprise reconfigurable execution nodes, as claimed.

In a further difference from the claim language, the Examiner reads the plurality of data buses again on cache memory MEM 8 and argues that all MEM 0 – MEM 8 are alike. This is incorrect. It can be seen by review of Figure 5, cited by the Examiner, that the output of MEM 8 runs only to the cross bar switch 51 and the processors 46 and 48. No other memory has such a connection. The remaining memories MEM 0 – MEM 7 are connected only to the transpose in-bus and the transpose out-bus. There is only a single line running from each memory to each of those buses. Therefore, these memories also do not meet the limitations of the claims, which require each of the plurality of cache memory units have a plurality of cache ports and that each and every

one of the cache port connected to each and every one of the buses. It is this plurality of connections which enables the control words, which are stored in the cache memory, and which are now clearly recited in amended claim 1, to be quickly withdrawn from separate lines in each of the memory units and conveyed to the RXN to control the configuration of the RXN. For these reasons, the Wilson reference does not teach the limitations of amended claim 1.

As to claims 3 and 4, which depend from claim 1, the Examiner cites the multiplexers appearing in Figure 7 of Wilson. However, as previously noted, these multiplexers are simple the detailed logic incorporated in truth data processor 48, which does not receive outputs of all the memories MEM 0 – MEM 7. There is no teaching that these multiplexers can be used, or adapted to be used, to selectively convey control words from the cache memory to an RXN or a processor similar to the RXN as claimed.

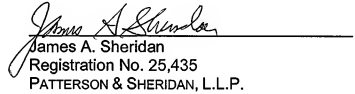
The Examiner is further directed to claims 7 and 8, which are also not taught by Wilson, since Wilson does not teach a connection from a plurality of busses to a plurality of ports of every memory unit. The Examiner also cites the abstract of Wilson. But this teaches only that sequential bursts of consecutive rows from a data matrix may be transferred. Specifically, once a first address of a sequence of rows is identified, the following members of the burst are "sequentially" transferred. The abstract does not teach, as claimed herein, that line a from each of the plurality of cache memory units is simultaneously transferred over each of a plurality of buses to the RXN to selectively control the RXN.

These same arguments clearly distinguish teachings of Wilson from the limitations of claims 12 and 20. Each of these claims requires that each of the memory units comprises a plurality of lines and that each and every one of these lines is connected to each and every one of the plurality of buses, which are made available in the processing node. In Wilson, each of the memory units MEM 0 – MEM 7 has, at most, two connections to the plurality of data buses, and this number of connections is clearly less than the number of memory units and the number of buses. The reference clearly teaches that there are 8 memory units and that there are 8 in-buses and 8 out-buses, but each memory unit has only one connection to the in-bus and one connection

to the out-bus. Therefore, the structure recited in claims 12 and 20, and the simultaneous transfer of data values from each and every one of the memory units to each and every one of the bus lines, are not taught or achievable with the structure proposed by Wilson.

The Examiner has not relied on Okuda against these claims, but a review of Okuda clearly establishes that it does not make up for the deficiencies of the Wilson reference. Therefore, reconsideration and allowance of these claims are respectfully requested.

Respectfully submitted,



James A. Sheridan
Registration No. 25,435
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)